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Harmonic-Recycling Rectification Based on Novel Compact Dual-Band Resonator

基于新型紧凑双频谐振器的谐波回收整流

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***Abstract*—Harmonic generation during RF-DC conversion causes performance degradation of a microwave rectifying circuit. To suppress and recycle the harmonic power, this letter proposes a novel compact dual-band resonator (DBR) based on a microstrip coupled transmission line. It presents open-circuits at the second and third harmonic frequencies, which effectively block the higher-order harmonic for power recycling. The conventional input cascading filters for harmonic rejection can be eliminated, simplifying the circuit topology and reducing loss. Theoretical analyses were carried out and corresponding equations were formulated for the proposed DBR. For validation, two rectifying circuits with/without the DBR operating at 2.2 GHz were fabricated and tested. Using the proposed DBR at 10 dBm RF power, the suppression of the second and third harmonic powers is enhanced by 18.4 dB and 7.6 dB, respectively. Besides, an improvement of RF-DC power efficiency (PCE) was observed; specifically, PCE reached 73.2% at 10 dBm compared to 71.6% obtained from an equivalent rectifier.**

摘要——谐波在射频-直流转换过程中产生，会导致微波整流电路的性能下降。为抑制并回收谐波功率，本文提出一种基于微带耦合传输线的新型紧凑双频谐振器（DBR）。该谐振器基于微带耦合传输线。它在二次和三次谐波频率处呈现开路，可有效阻断高次谐波以实现功率回收。传统的用于谐波抑制的输入级联滤波器可以省去，从而简化电路拓扑并降低损耗。本文对所提出的DBR进行了理论分析并推导了相应方程。为验证该方案，制作并测试了两种在 2.2 GHz 下工作的整流电路，分别采用和未采用 DBR。在 10 分贝毫瓦射频功率下，采用提出的 DBR 后，二次和三次谐波功率的抑制分别提升了 18.4 dB 和 7.6 dB。此外，射频-直流功率效率（功率转换效率，PCE）也有所提升，具体而言，在 10 分贝毫瓦下，PCE 达到 73.2%，而等效整流器的 PCE 为 71.6%。

***Index Terms*—Dual-band resonator, harmonic-recycling, rectifying circuit, wireless power transmission**

索引术语——双频谐振器，谐波回收，整流电路，无线电力传输

I. INTRODUCTION

I. 引言

MICROWAVE rectifying circuits, essential components in wireless power transmission (WPT) systems, play a crucial role in converting RF power to DC power [1], [2], [3].

微波整流电路是无线电力传输（WPT）系统中的关键组件，在将射频功率转换为直流功率方面发挥着重要作用[1]，[2]，[3]。

The overall efficiency of wireless power transfer (WPT) systems heavily relies on the power conversion efficiency (PCE) of the rectifying circuit [4], [5], [6], [7]. Therefore, the primary requirement of a rectifying circuit is high RF-DC power conversion efficiency (PCE), and miniaturization is another requirement for system integration in the antenna array.

无线电力传输（WPT）系统的整体效率很大程度上取决于整流电路的功率转换效率（PCE）[4]，[5]，[6]，[7]。因此，整流电路的首要要求是具有较高的射频-直流功率转换效率（PCE）；此外，为了实现天线阵列的系统集成，还需满足小型化要求。

In a rectifying circuit, the diode generates frequency harmonics from the incoming power, thereby reducing the proportion of energy converted to direct current and resulting in unwanted harmonic emissions. Moreover, as the incident radio frequency (RF) energy increases, the energy lost to harmonics further increases [8], [9]. Consequently, recycling rectification of the harmonic power is an effective method to boost the PCE of a rectifying circuit.

在整流电路中，二极管会将输入功率中的能量转化为频率谐波，从而减少转换为直流电的能量比例，并产生不需要的谐波辐射。此外，随着入射射频（RF）能量增加，谐波造成的能量损失也会进一步增加 [8]，[9]。因此，回收谐波功率进行整流，是提高整流电路功率转换效率的有效方法。

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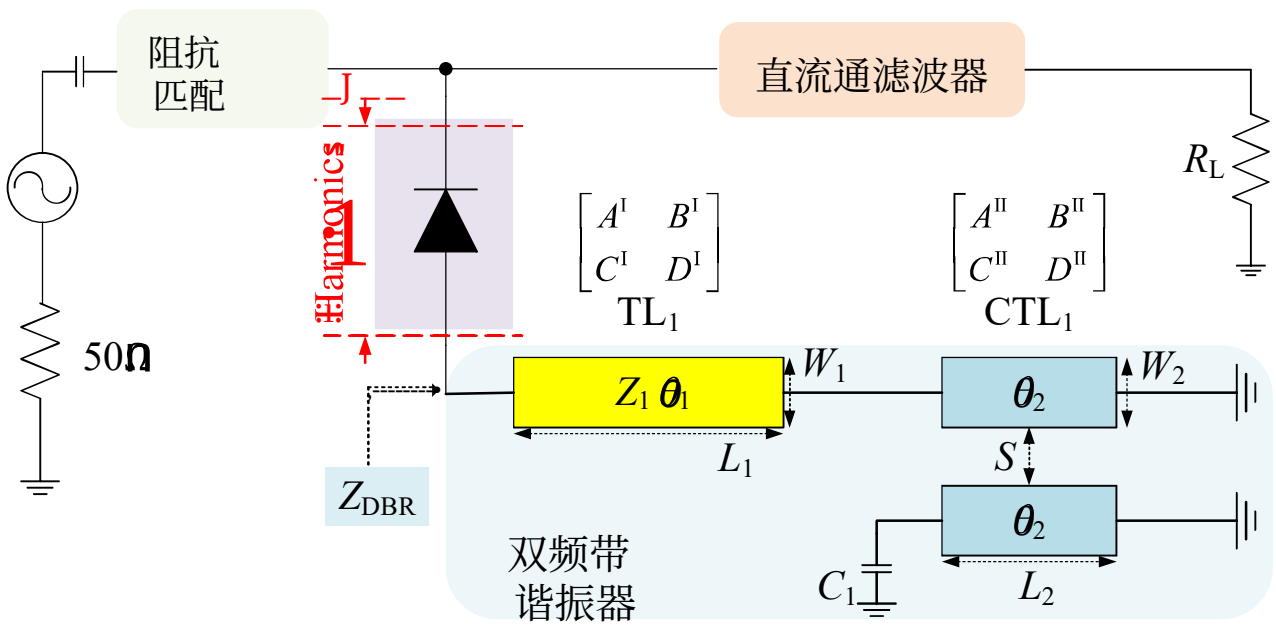

Fig. 1. A microwave rectifying circuit using a DBR for harmonic recycling.

图1. 采用DBR进行谐波回收的微波整流电路。

Filtering of the harmonics at both the input and output has been investigated, as shown in [10] and [11], mainly to reduce re-radiated harmonic power. Usually, filters, e.g., band-stop [12] or low-pass filter [13] are applied between the diodes and the input/output of the microwave rectifier to reflect harmonics produced during rectifying, and the reflected harmonics go back to the diode where they can be converted to DC. It is noticed that the filters at the input raise a concern about the insertion loss and circuit area.

如[10]和[11]所示，已研究在输入端和输出端对谐波进行滤波，主要目的是降低再辐射谐波功率。通常，在二极管与微波整流器的输入端/输出端之间使用滤波器，例如带阻[12]或低通滤波器 [13]，以反射整流过程中产生的谐波；反射回去的谐波会返回二极管，并在其中转换为直流。值得注意的是，输入端的滤波器会引发对插入损耗和电路面积的担忧。

Class-F loads and harmonic-terminated techniques are alternatives to the low-pass or dc-pass of rectifiers [14], it has good potential applications for high-frequency microwave rectifiers. Diode rectifiers using Class-C loads [15], [16] and a 5.8-GHz charge pump rectifier with Class-F loads [17] demonstrated an improvement in PCE. In reality, the optimum impedance for harmonic-terminated operation is difficult to achieve as the package of the device has parasitics that move the harmonic impedances.

C类负载和谐波终端技术是整流器低通或直通方案的替代方案[14]，，在高频微波整流器中具有良好的应用潜力。采用C类负载的二极管整流器[15]，[16]以及采用F类负载的5.8 GHz电荷泵整流器 [17]均实现了功率转换效率的提升。实际上，由于器件封装中的寄生参数会改变谐波阻抗，因此难以实现谐波终端工作所需的最佳阻抗。

Recently, a competitive solution has emerged in the form of a compact serial bandstop structure. This innovative approach not only effectively blocks radiation of harmonics but also compensates for the diode capacitive impedance at the fundamental frequency [7], [18]. In [7], a short-ended eighth-wavelength microstrip transmission line was employed to impede the second harmonic and enhance power recycling. However, solely the second harmonic can be recycled.

近期，一种具有竞争力的解决方案——紧凑型串联带阻结构应运而生。这种创新方法不仅能有效阻断谐波辐射，还能补偿基波频率下的二极管容性阻抗 [7]，[18]。在 [7]中，采用了一条短端接的八分之一波长微带传输线来抑制二次谐波并增强功率回收。然而，这种方法只能回收二次谐波。

In this letter, we propose a novel harmonic suppression structure using a dual-band resonator (DBR) to efficiently recycle both the second and third harmonic power with a compact circuit topology. The DBR is based on our previous work [19], where we found that a microstrip line in serial with a coupled pair of microstrip-lines could provide two poles (open-circuits) for impeding harmonic radiation. In this letter, we further investigate this structure as a DBR to demonstrate its ability to block the second and third harmonics for enhanced power recycling compared to [7]. With the proposed DBR, a simple and compact circuit structure was realized, resulting in a decrease in insertion loss and an improvement of PCE.

本文提出一种新型谐波抑制结构，采用双频谐振器（DBR）以紧凑的电路拓扑高效回收二次和三次谐波功率。该DBR基于我们先前的研究[19]，，我们在其中发现，与一对耦合微带线串联的微带线可提供两个极点（开路），以抑制谐波辐射。本文进一步研究了该结构作为DBR的应用，并证明与[7]相比，它能够阻断二次和三次谐波，从而提升功率回收效果。采用所提出的DBR，实现了简单紧凑的电路结构，降低了插入损耗并提高了功率转换效率（PCE）。

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II. Principle and Design Method

A. Principle

As shown in Fig. 1, owing to the high impedance provided by the harmonic suppression structure, high-order harmonics are confined to the diode without returning to the input port, thus the conversion efficiency of a rectifying circuit can be improved. However, in this design, the harmonic suppression structure in series with the diode has been realized through a DBR which is placed between the diode and the ground plane. A DBR in series with the diode should have the following functions:

1) Presenting a short circuit at DC, which provides a DC path for the rectifying circuit output.
2) Compensating the capacitive impedance of the diode, which facilitates the impedance matching circuit of the rectifying circuit.
3) Exhibiting high reflections at harmonic frequencies nf (n 3), which blocks them from returning the input port.

Fig. 1 shows a rectifying circuit operating with a DBR for harmonic recycling. It has three parts: 1) a quarter-wave transformer, which may be needed for the impedance matching at f_0; 2) a DC-pass filter to prevent RF signals from entering the load; 3) a DBR, employed to recycle the second and third harmonic power through rectifying or mixing with other frequencies.

B. The proposed DBR

Based on the above analysis, the input impedance of the proposed DBR for harmonic recycling can be expressed as

$$\begin{cases} Z_{\mathrm{DBR}}@\mathrm{DC} = 0 \\ Z_{\mathrm{DBR}}@f_0 = jX_L \\ Z_{\mathrm{DBR}}@2f_0 = \infty \\ Z_{\mathrm{DBR}}@3f_0 = \infty \end{cases} \tag{1}$$

A practical microstrip band-stop structure to block the third harmonics is a short-ended $\lambda/12$ transmission line. Inspired by this idea, a small section of a short-ended $\lambda/12$ transmission line is modified with a coupled transmission line (CTL), which is shown Fig. 1. Due to the odd and even modes of the CTL, besides the third harmonic, another resonant frequency at the second harmonic can be simultaneously obtained.

Fig. 1 shows the schematic of the proposed DBR. The impedance and electrical length of TL are Z and , respectively, thus its ABCD matrix [20] is

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cos\theta_1 & jZ_1\sin\theta_1 \\ j\frac{\sin\theta_1}{Z_1} & \cos\theta_1 \end{bmatrix}. \tag{2}$$

Width W_2 and gap S determine the even- and odd-mode impedance of CTL, Z_{0e} and Z_{0d}. The ABCD matrix of CTL_1 can be expressed as

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \frac{Z_{0e}+Z_{0d}}{Z_{0e}-Z_{0d}} & j\frac{2\tan\theta_2}{(Z_{0e}-Z_{0d})} \\ -j\frac{2\cot\theta_2}{Z_{0e}-Z_{0d}} & \frac{Z_{0e}+Z_{0d}}{Z_{0e}-Z_{0d}} \end{bmatrix}. \tag{3}$$

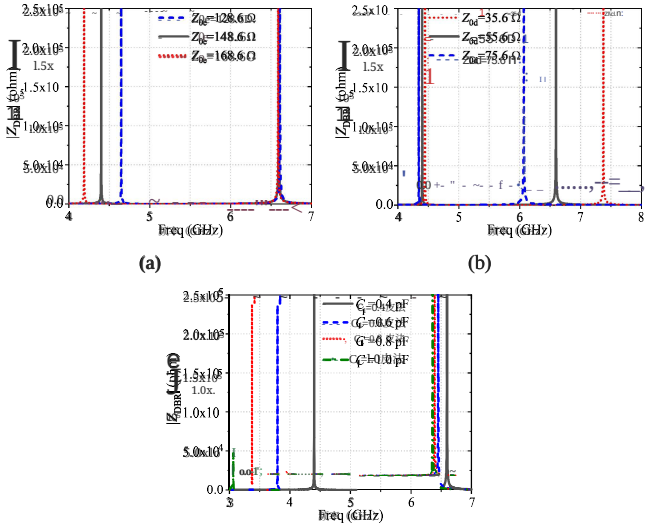

Fig. 2. Calculated $|Z_{\mathrm{DBR}}|$ versus RF frequency with perturbation of (a) Z_{0e}. (b) Z_{0d}. (c) C_1.

Cascading (2) of ABCD matrices and Equation (2) and (3) leads to

$$\begin{bmatrix} A^{\mathrm{III}} & B^{\mathrm{III}} \\ C^{\mathrm{III}} & D^{\mathrm{III}} \end{bmatrix} = \begin{bmatrix} A^{\mathrm{I}} & B^{\mathrm{I}} \\ C^{\mathrm{I}} & D^{\mathrm{I}} \end{bmatrix} \times \begin{bmatrix} A^{\mathrm{II}} & B^{\mathrm{II}} \\ C^{\mathrm{II}} & D^{\mathrm{II}} \end{bmatrix}. \tag{4}$$

Finally, the input impedance of the proposed DBR with one port terminated in C, is

$$Z_{\mathrm{DBR}} \equiv \frac{A^{\mathrm{III}}Z_C + B^{\mathrm{III}}}{C^{\mathrm{III}}Z_C + D^{\mathrm{III}}} \tag{5}$$

where, Z_C is the impedance of capacitor C_1.

To verify the input impedance calculation and the performance of the proposed DBR, numerical experiments were carried out for a DBR operating at a fundamental frequency of 2.2 GHz. Considering the fabrication precision of PCB manufacture, the default width W and gap S of CTL_1 are 0.3 mm and 0.2 mm, respectively. Since TL_1 is wider than CTL_1, its width W_1 stays the same as W. Thus, the initial parameters of DBR are $Z_1 = 107.6\ \Omega$, $Z_{0e} = 148.6\ \Omega$, and $Z_{0d} = 55.6\ \Omega$ with an RF laminate RO4350B of 0.76-mm thickness. When C is 0.4 pF, and are calculated as 15.9 and 18.6°, respectively. Substituting the above parameters into (5) for calculation, Fig. 2 shows the calculated $|Z_{\mathrm{DBR}}|$ with perturbation of Z_{0e}, Z_{0d}, and C, respectively.

Through sweeping each parameter individually, as shown in Fig. 2(a), the first pole of $|Z_{\mathrm{DBR}}|$ shifts to the left side dynamically with an increase of Z_{0e}, whereas the second pole of $|Z_{\mathrm{DBR}}|$ moves to the right side rapidly with a decrease of Z_{0d} (see Fig. 2(b)). Regarding the influence of capacitor C, Fig. 2(c) illustrates the shift in $|Z_{\mathrm{DBR}}|$ as C increases towards infinity (effectively a short circuit), with the other parameters remain the same as those in Fig. 2(a). It is observed the second pole of $|Z_{\mathrm{DBR}}|$ stays the same place because C is equivalent to a short circuit at a relatively high frequency, whereas the first pole shifts towards lower frequencies as C increases. As a result, the first pole can be tuned through C. However, a large C may place the first pole very close to f_0, which should be avoided.

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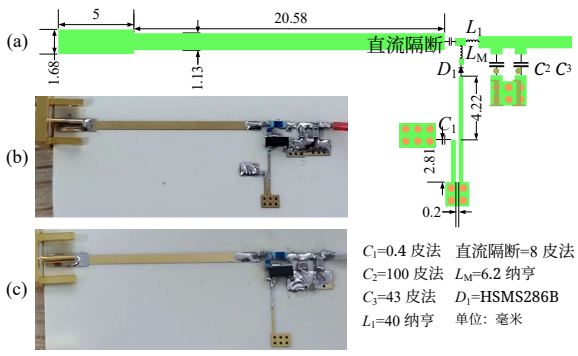

Fig3. (a) Circuit layout with design parameters for the proposed DBR. (b) A rectifying circuit with the proposed DBR. (c) A rectifying circuit without harmonic recycling for performance comparison.

图3. (a) 所提出 DBR 的电路布局及设计参数。(b) 采用所提出 DBR 的整流电路。(c) 不进行谐波回收的整流电路，用于性能比较。

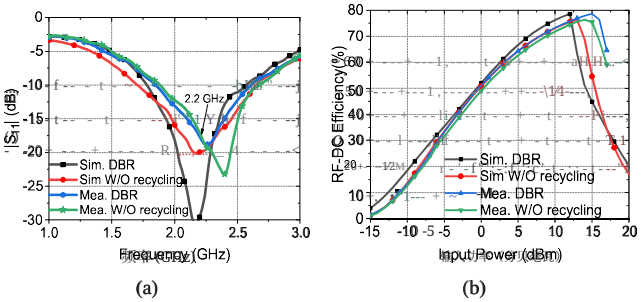

Fig. 4. (a) Simulated and measured $|S_{11}|$ versus RF frequency at 10-dBm input power and (b) PCE versus RF input power.

图4. (a) 在输入功率为 10 分贝毫瓦时，$|S_{11}|$ 随射频频率变化的模拟和实测值。(b) 功率转换效率随射频输入功率的变化。

III. Implementation and Measurement

A rectifying circuit (Fig. 3) operating at f_0 = 2.2 GHz was simulated in Advanced Design System (ADS, Keysight) with physical dimensions indicated in Fig. 3, and the RO4350B (ϵ_r = 3.66 and $\tan\delta$ = 0.002) was used. L_M is a chip inductor for compensating the capacitive impedance of the diode. Fig. 3 shows a photograph of the fabricated rectifying circuit. For performance comparison, a rectifying circuit without harmonic recycling was also fabricated.

The measured reflection coefficient $|S_{11}|$ at the input power of 0 and 10 dBm are shown in Fig. 4(a). For the rectifying circuit with the DBR, $|S_{11}|$ curve for 10 dBm is well below -10 dB for frequencies ranging from 1.85 to 2.6 GHz. It is observed that $|S_{11}|$ for rectifying circuits with/without the DBR are almost the same.

Fig. 4(b) depicts the simulated and measured PCE versus input power at 2.2 GHz and 400-Ω DC load. As observed at 10 dBm, the measured PCE of the rectifying circuits with/without the proposed DBR are 73.2% and 71.6% respectively, while simulated PCE for both rectifiers are 76.2% and 73.4%, respectively. Because the measured $|S_{11}|$ versus input power are not much different for both rectifiers, the improvement in PCE by the measurement is lower than that of the simulation. Compared to the reference rectifier, the rectifying circuit using the proposed DBR shows an improvement in PCE at high input power levels (6 to 14 dBm).

The measured power levels of the second and third harmonic are depicted in Fig. 5(a), where the rectifying circuit with DBR presents an obvious low point at 2.2 GHz. Specifically, at 10 dBm, the suppression of the second harmonic is enhanced from 6.7 dBm to 25.1 dBm by the proposed DBR (an improvement of 18.4 dB). Meanwhile, as shown in Fig. 5(b), the rectifying circuit with DBR demonstrates better control over the third harmonic, showing an improvement of 7.6 dB by comparison. The measured harmonic power versus frequency validates the effectiveness of harmonic control through the proposed DBR.

Table I shows a comparison of the performance between the proposed rectifying circuit and those reported in the literature targeting harmonic recycling. As shown, the rectifying circuit using the proposed DBR has demonstrated the effectiveness of harmonic control over the second and third harmonics, while harmonic suppressions in other references were not reported. Meanwhile, only one diode is used, which helps to minimize the losses associated with the diode turn-on voltage.

IV. Conclusion

A novel compact dual-band resonator (DBR) has been developed for recycling the second and third harmonic power in a microwave rectifying circuit. It functions as both a filter and an inductor for impedance matching, the conventional input cascading band-pass or low-pass filters for harmonic rejection can be eliminated, leading to a simple circuit topology with low loss. Compared to a reference rectifier, the proposed DBR demonstrates better control over the second and third harmonic, showing an improvement of 18.4 dB and 7.6 dB respectively. Besides, improved PCEs at high input power levels were also observed.

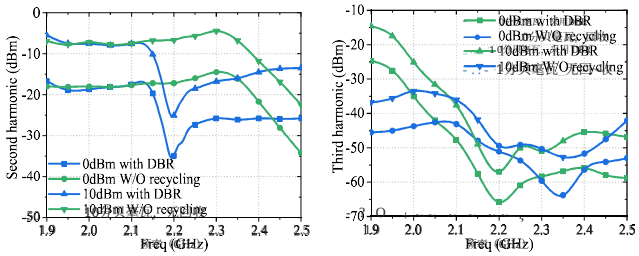

Fig. 5. Measured harmonic power versus RF frequency at 0- and 10-dBm input power. (a) Second harmonic. (b) Third harmonic.

图5. 输入功率为 0 和 10 分贝毫瓦时测得的谐波功率与射频频率的关系。(a) 二次谐波。(b) 三次谐波。

TABLE I
PERFORMANCE COMPARISON OF HARMONIC-RECYCLING RECTIFIERS

表I 谐波回收整流器性能比较

Ref.	[7]	[18]	[21]	This work
Freq (GHz)	2.45	2.45	2.6	2.2
PCE (%)	80.9	80.2	47	78.6
Pow.(dBm)	20	25	0	15
Diode	HSMS-282	HSMS-282	HSMS-2850,2860	HSMS-286B
Size (mm)	16×18	20×55	37×31	34×11
Size (λ_g^2)	0.051	0.018	0.219	0.073
Technology	TL A/S shorted	TL A/S shorted	Another rectifier cell	Dual-band resonator
Harmonic Supp. (dB)	N.A	N.A	N.A	18.4@$2f_0$ 7.6@$3f_0$
Diode Num.	1	2	2	1

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